PRESS RELEASE

**Lauterbach and Kernkonzept Enable Development of Virtualized RISC-V Systems**

Hoehenkirchen and Dresden, Germany – 14th October 2024. As the industry's first supplier, Lauterbach and Kernkonzept enable architects of virtualized software systems to start development and testing on future RISC-V platforms, even before corresponding System-on-Chips (SoCs) are available in silicon.

To execute mixed-critical workloads with different security levels on a high-performance processor, strong isolation including the respective operating systems is essential. To achieve this, developers can virtualize the underlying hardware with the help of a hypervisor, whereby workloads with different safety levels are executed in isolated Virtual Machines (VMs).

A software architecture for Software-Defined-Vehicles (SDV) for example combines cloud technologies with automotive functional safety and real-time requirements for the first time, with the consequence that virtualization is indispensable. Leading semiconductor suppliers in the automotive value chain have already committed to RISC-V. However, corresponding SoCs, which will enable virtualization on RISC-V CPUs, are still under development.

In order to give developers the opportunity to create appropriate software right now, Kernkonzept and Lauterbach enable for the first time the development, debugging and testing of RISC-V software for virtualized software architectures on the well-known and widely used emulation platform QEMU.

For this, Kernkonzept’s leading-edge and proven L4Re Hypervisor runs on the Generic RISC-V Virtual Platform implemented in QEMU, while Lauterbach’s TRACE32® debug and trace tools allow the analysis of the entire software stack including the L4Re hypervisor itself and all virtual machines (VM) with their heterogeneous OSes and applications.

As a result, developers of virtualized software architectures and applications running on heterogeneous rich and real-time OSes can start their development work immediately, even before the corresponding RISC-V chips are delivered in silicon.

Kernkonzept’s L4Re Hypervisor securely separates real-time workloads, even on very small chips. The minimal code base in privileged mode and all its possibilities for integrating security and safety functions perfectly into the system make the L4Re Hypervisor family ideally suited for products that must be certified. By leveraging these features, the risk in the certification process is significantly reduced, while also saving time and resources. This makes it the perfect application for the automotive industry, avionics, or the IoT. By combining the open-source software L4Re with the open architecture RISC-V, Kernkonzept can provide more customers with state-of-the-art security software, enhancing their system integrity.

TRACE32® enables simultaneous debugging of the CPU and other cores in an emulated or silicon SoC, a unique capability that covers the entire system. On virtualized systems, TRACE32® Hypervisor-aware debugging allows to perform concurrent OS-aware debugging for each guest OS/virtual machine (VM) and display an overview of the overall system. TRACE32® tools provide access to hypervisor and OS structures and data, so developers can better understand how they are behaving and utilizing chip resources.

“We are excited to enable the development of virtualized software architectures on RISC-V together with Kernkonzept”, said Norbert Weiss, Managing Director of Lauterbach GmbH. “Virtualization is the key to Software Defined Vehicles, where multiple safety-critical and non-critical applications are sharing a platform and thanks to our collaboration, developers can start creating world-class software immediately”, said Adam Lackorzynski, founder and CTO at Kernkonzept.

As technology leaders in their respective fields, Lauterbach and Kernkonzept support virtualized software architectures for RISC-V from the very beginning.

Find more about Kernkonzept’s L4Re Hypervisor: <https://www.kernkonzept.com/l4re-operating-system-framework/>

Find more about Lauterbach’s Hypervisor- and OS-Awareness technology: <https://www.lauterbach.com/features/os-awareness>

Find more about the QEMU emulation platform: <https://www.qemu.org/>

Kernkonzept is a specialist in secure and safe virtualization and operating-system technology. Our customers build complex software products for safety-, security-, and mission-critical applications, often requiring certification or accreditation. Based on our open-source L4Re technology – a microkernel-based operating-system and hypervisor platform – we engineer system solutions with a minimal attack surface, real-time capabilities, and virtualization support. Our deeply experienced operating-system engineers tailor these solutions to the needs of the automotive, high-assurance-security, and embedded markets and furthermore they provide our customers with comprehensive and personal architectural consulting. Kernkonzept GmbH is an SME based in Dresden, Germany.

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**Lauterbach** is the leading manufacturer of cutting-edge development tools for embedded systems with more than 40 years of experience. The company has played a key role in the RISC-V Foundation working groups that have defined debug and trace standards for RISC-V-based CPUs. Lauterbach is an international, well-established company, serving customers all over the world, partnering with all semiconductor manufacturers and growing steadily. At the headquarters in Hoehenkirchen, near Munich, the engineering team develops and produces highly proficient and specialized, easy-to-use Development Tools under the brand TRACE32®. Branch offices in United Kingdom, Italy, France, Tunisia, on the East and West coasts of the United States, Japan and China and highly qualified sales as well as support engineers in many other countries make Lauterbach’s full product range available worldwide.

For more information, please visit http://www.lauterbach.com/

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